

# DATA SHEET

## **74F821/822/823/824/825/826** Bus interface registers

Product specification

1996 Jan 05

IC15 Data Handbook

## Bus interface registers

## 74F821/822/823/824/825/826

- 74F821 10-bit bus interface register, non-inverting (3-State)  
 74F822 10-bit bus interface register, inverting (3-State)  
 74F823 9-bit bus interface register, non-inverting (3-State)  
 74F824 9-bit bus interface register, inverting (3-State)  
 74F825 8-bit bus interface register, non-inverting (3-State)  
 74F826 8-bit bus interface register, inverting (3-State)

### FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- High performance bus interface buffering for wide data/address paths or busses carrying parity
- High impedance PNP base inputs for reduced loading (20 $\mu$ A in high and low states)
- $I_{IL}$  is 20 $\mu$ A vs 1000 $\mu$ A for AM29821 series
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan-in as required with MOS microprocessor
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- Slim Dip 300 mil package
- Broadside pinout compatible with AMD AM 29821-29826 series
- Outputs sink 64mA and source 24mA
- Industrial temperature range available (-40°C to +85°C) for 74F823

### DESCRIPTION

The 74F821 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of busses carrying parity.

The 74F821/74F822 are buffered 10-bit wide versions of the popular 74F374/74F534 functions.

The 74F822 is the inverted output version of 74F821.

The 74F823 and 74F824 are 9-bit wide buffered registers with clock enable ( $\overline{CE}$ ) and master reset ( $\overline{MR}$ ) which are ideal for parity bus interfacing in high microprogrammed systems.

The 74F824 is the inverted version of 74F823.

The 74F825 and 74F826 are 8-bit buffered registers with all the 74F823/74F824 controls plus output enable ( $\overline{OE0}$ ,  $\overline{OE1}$ ,  $\overline{OE2}$ ) to allow multiuser control of the interface, e.g.,  $\overline{CS}$ , DMA, and RD/ $\overline{WR}$ . They are ideal for uses as an output port requiring high  $I_{OL}/I_{OH}$ .

The 74F826 is the inverted version of 74F825.

TYPE	TYPICAL $f_{max}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F821, 74F822	180MHz	75mA
74F823, 74F824	180MHz	70mA
74F825, 74F826	180MHz	65mA

### ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG. DWG. #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$	
24-pin plastic slim DIP (300mil)	N74F821N, N74F822N, N74F823N, N74F824N, N74F825N, N74F826N	I74F823N	SOT222-1
24-pin plastic SOL	N74F821D, N74F822D, N74F823D, N74F824D, N74F825D, N74F826D	I74F823D	SOT137-1

# Bus interface registers

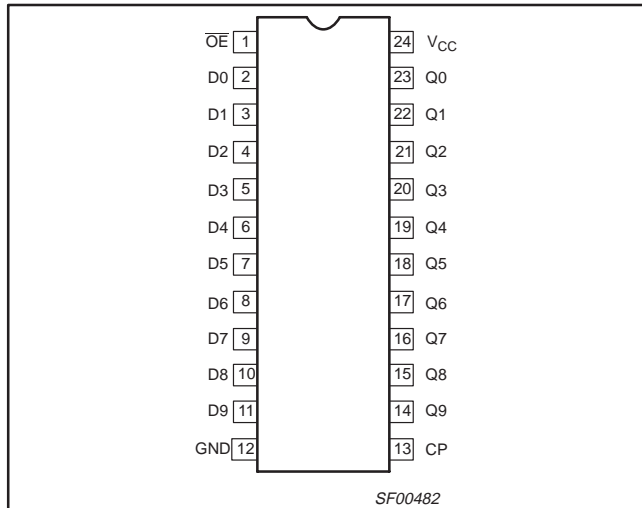
# 74F821/822/823/824/825/826

## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

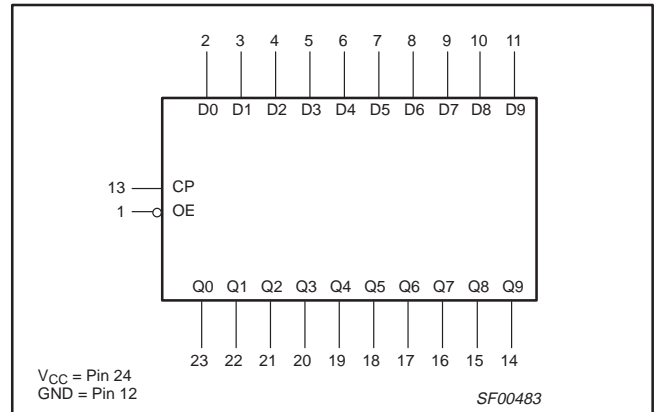
PINS		DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F821 74F822	Dn	Data inputs	1.0/1.0	20µA/0.6mA
	CP	Clock input	1.0/1.0	20µA/0.6mA
	$\overline{OE}$	Output enable input (active low)	1.0/3.0	20µA/1.8mA
	Qn, $\overline{Qn}$	Data outputs	1200/106.7	24mA/64mA
74F823 74F824	Dn	Data inputs	1.0/1.0	20µA/0.6mA
	CP	Clock input	1.0/1.0	20µA/0.6mA
	$\overline{CE}$	Clock enable input (active low)	1.0/3.0	20µA/1.8mA
	$\overline{MR}$	Master reset input (active low)	1.0/3.0	20µA/1.8mA
	$\overline{OE}$	Output enable input (active low)	1.0/3.0	20µA/1.8mA
	Qn, $\overline{Qn}$	Data outputs	1200/106.7	24mA/64mA
74F825 74F826	Dn	Data inputs	1.0/1.0	20µA/0.6mA
	CP	Clock input	1.0/1.0	20µA/0.6mA
	$\overline{CE}$	Clock enable input (active low)	1.0/3.0	20µA/1.8mA
	$\overline{MR}$	Master reset input (active low)	1.0/3.0	20µA/1.8mA
	$\overline{OE}$	Output enable input (active low)	1.0/3.0	20µA/1.8mA
	Qn, $\overline{Qn}$	Data outputs	1200/106.7	24mA/64mA

**NOTE:** One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

### PIN CONFIGURATION – 74F821



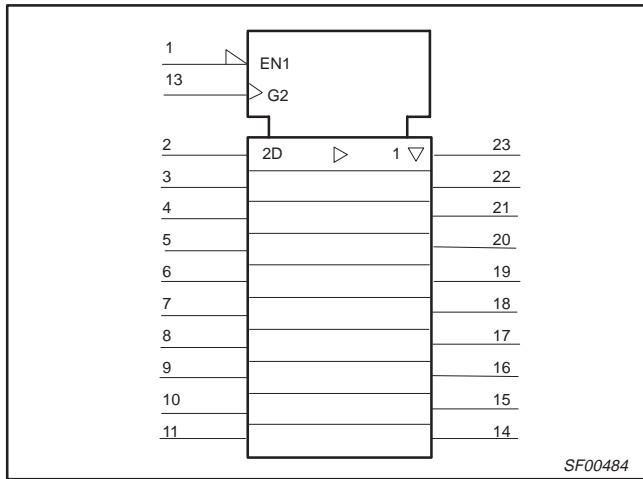
### LOGIC SYMBOL – 74F821



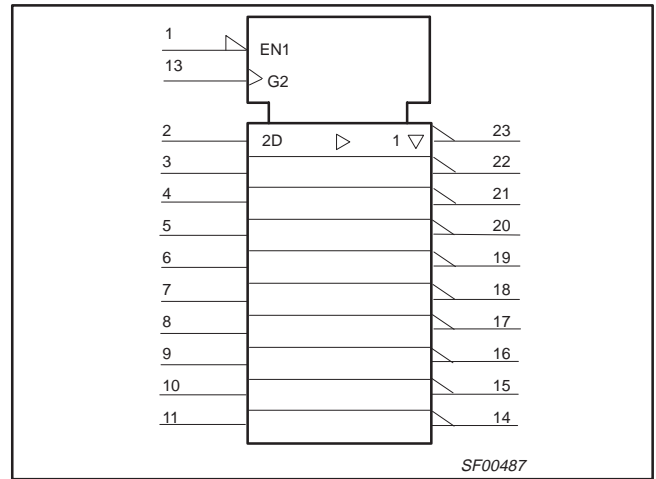
# Bus interface registers

# 74F821/822/823/824/825/826

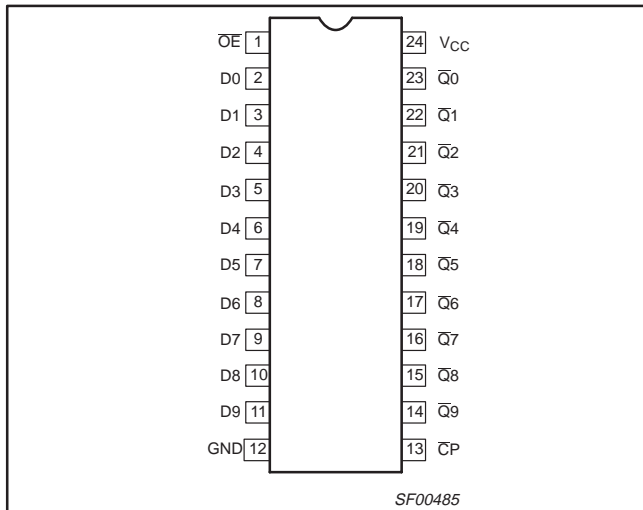
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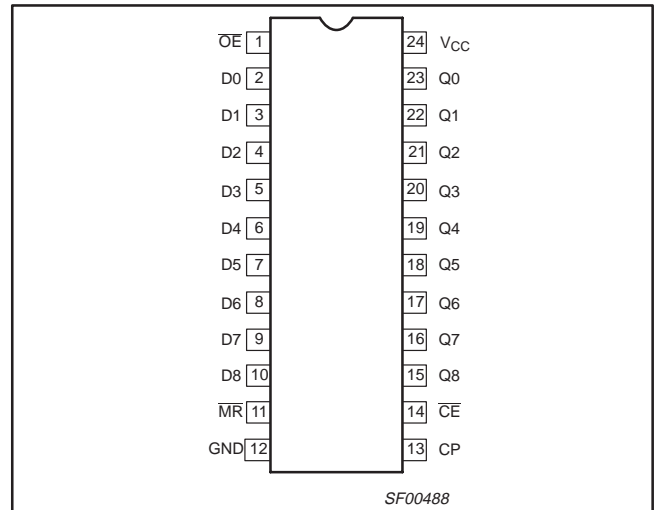
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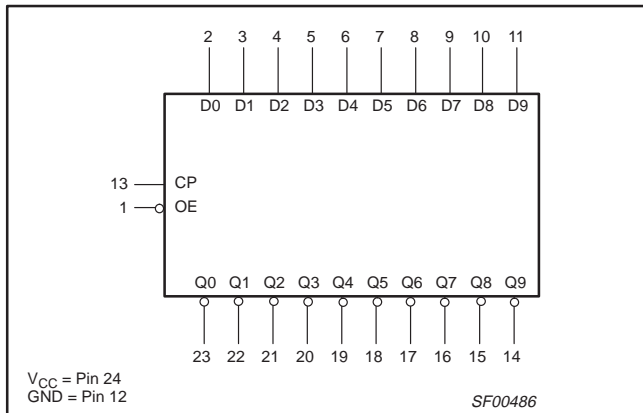
**PIN CONFIGURATION – 74F822**



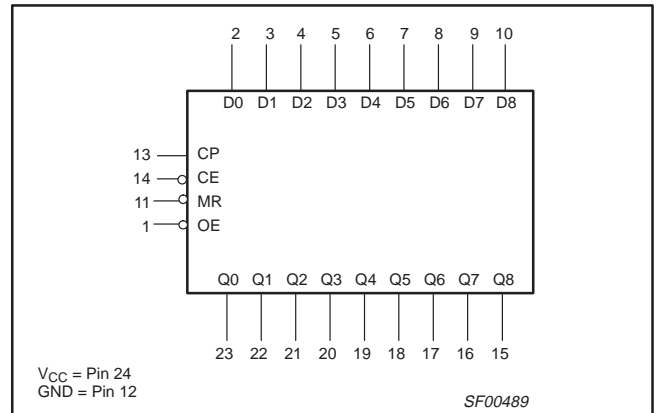
**PIN CONFIGURATION – 74F823**



**LOGIC SYMBOL – 74F822**



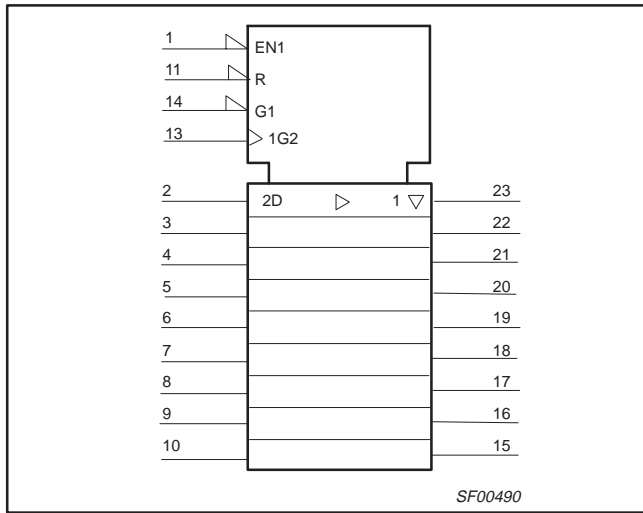
**LOGIC SYMBOL – 74F823**



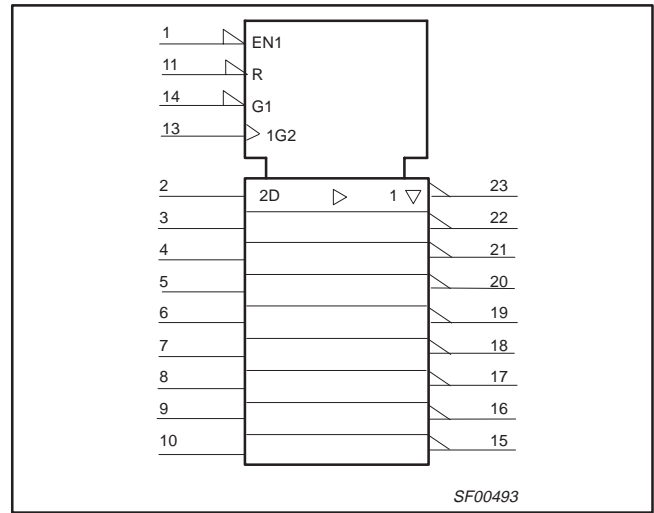
# Bus interface registers

# 74F821/822/823/824/825/826

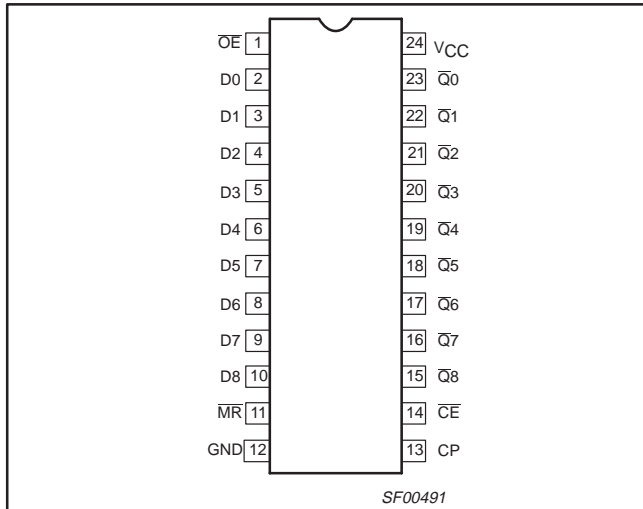
## IEC/IEEE SYMBOL – 74F823



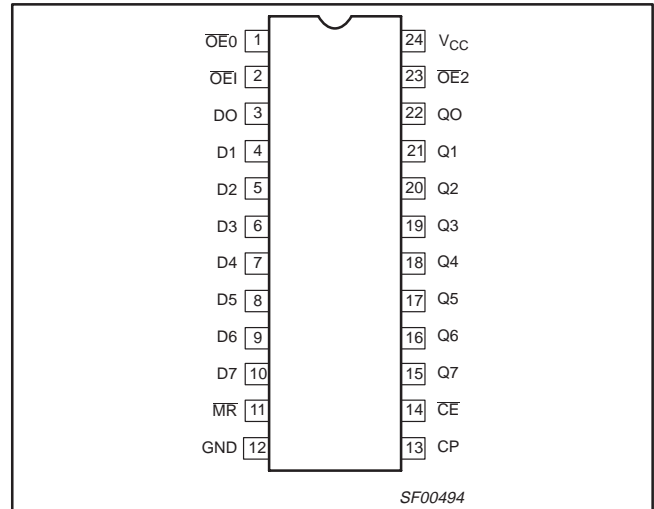
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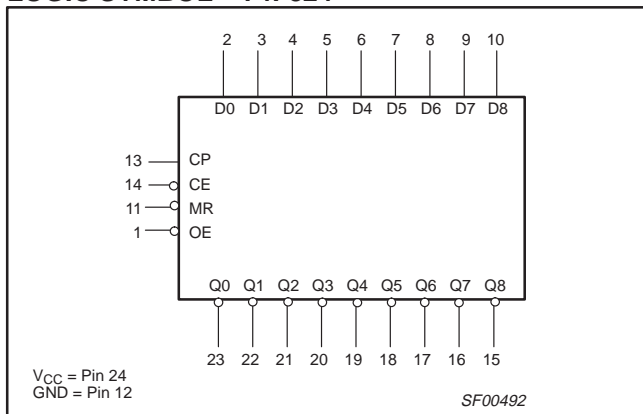
## PIN CONFIGURATION – 74F824



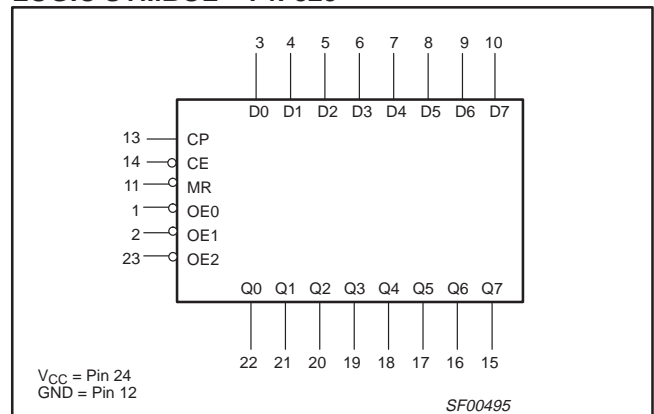
## PIN CONFIGURATION – 74F825



## LOGIC SYMBOL – 74F824



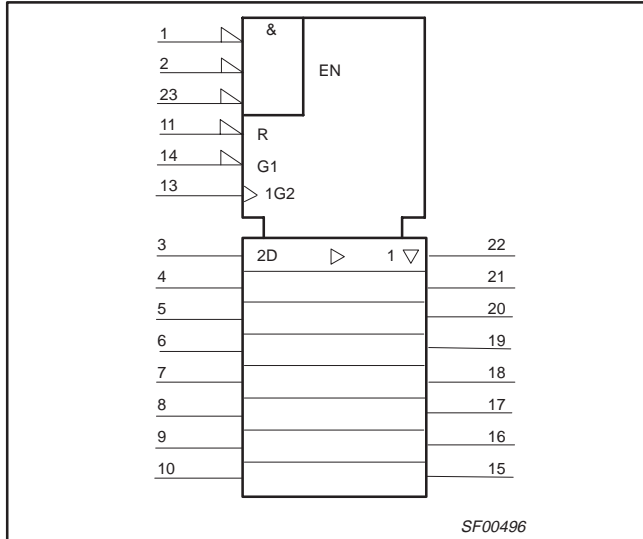
## LOGIC SYMBOL – 74F825



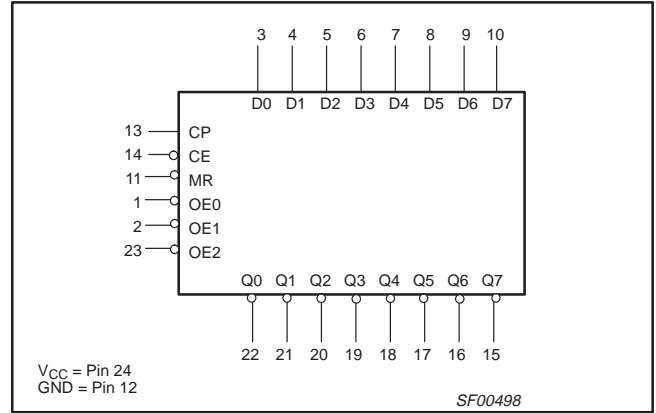
# Bus interface registers

# 74F821/822/823/824/825/826

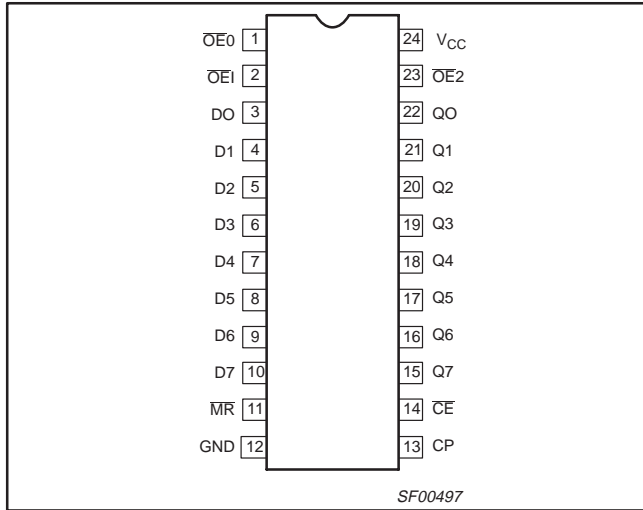
**IEC/IEEE SYMBOL – 74F825**



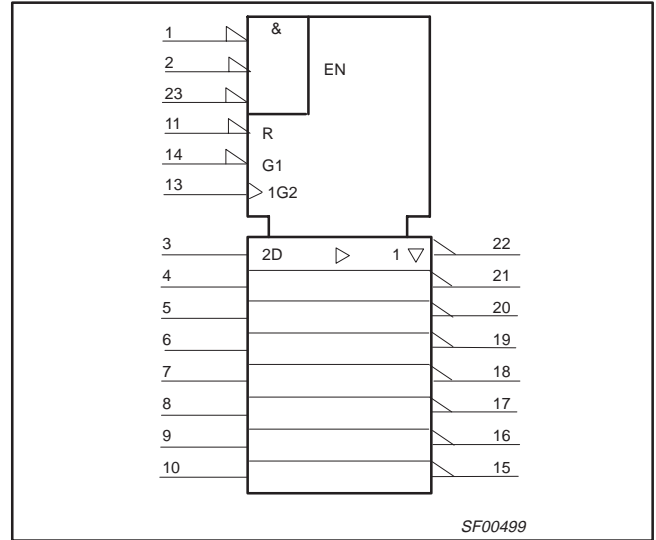
**LOGIC SYMBOL – 74F826**



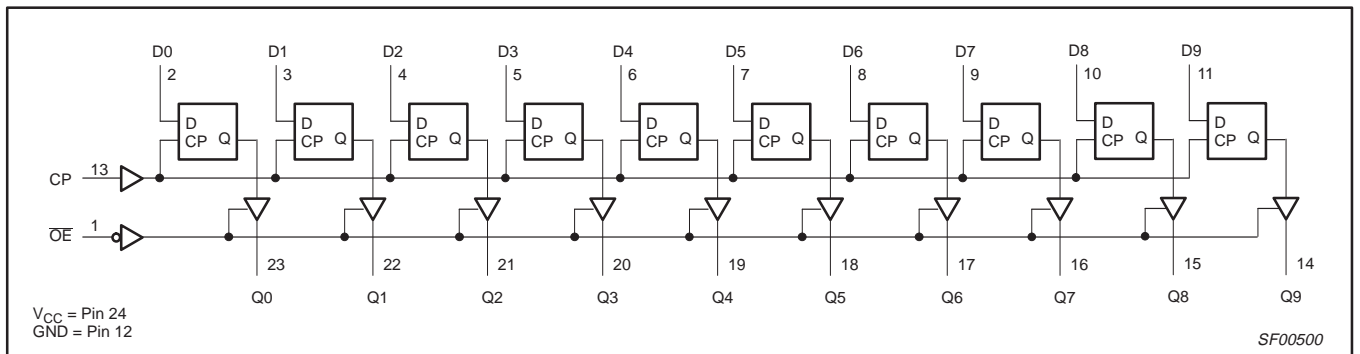
**PIN CONFIGURATION – 74F826**



**IEC/IEEE SYMBOL – 74F826**



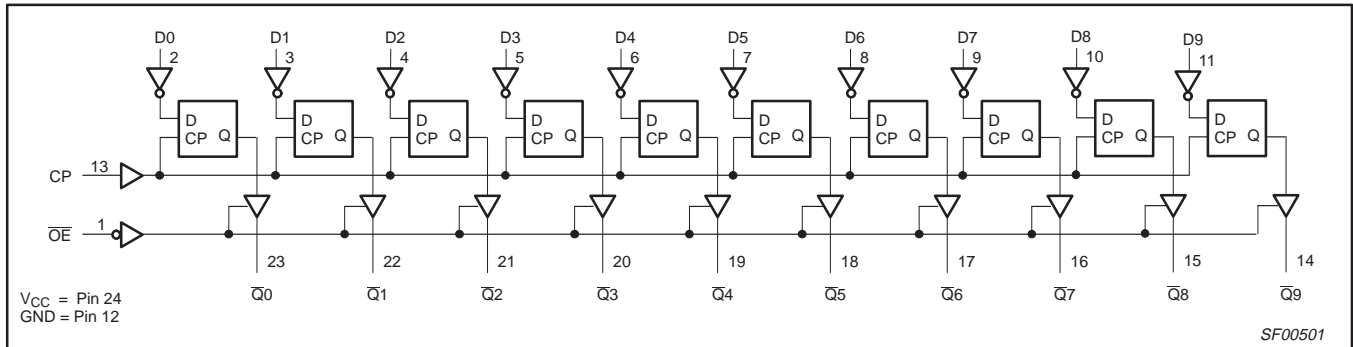
**LOGIC DIAGRAM FOR 74F821**



# Bus interface registers

## 74F821/822/823/824/825/826

### LOGIC DIAGRAM FOR 74F822

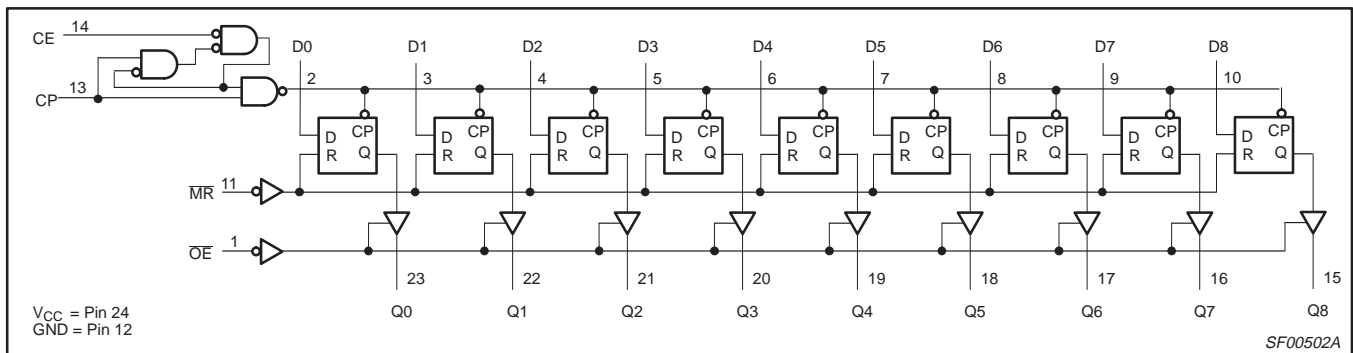


### FUNCTION TABLE FOR 74F821 AND 74F822

INPUTS			OUTPUTS		OPERATING MODE
			74F821	74F822	
OE	CP	D <sub>n</sub>	Q	Q̄	
L	↑	l	L	H	Load and read data
L	↑	h	H	L	
L	↕	X	NC	NC	Hold
H	X	X	Z	Z	High impedance

- H = High-voltage level
- h = High state must be present one setup time before the low-to-high clock transition
- L = Low-voltage level
- l = Low state must be present one setup time before the low-to-high clock transition
- NC = No change
- X = Don't care
- Z = High impedance "off" state
- ↑ = Low-to-high clock transition
- ↕ = Not low-to-high clock transition

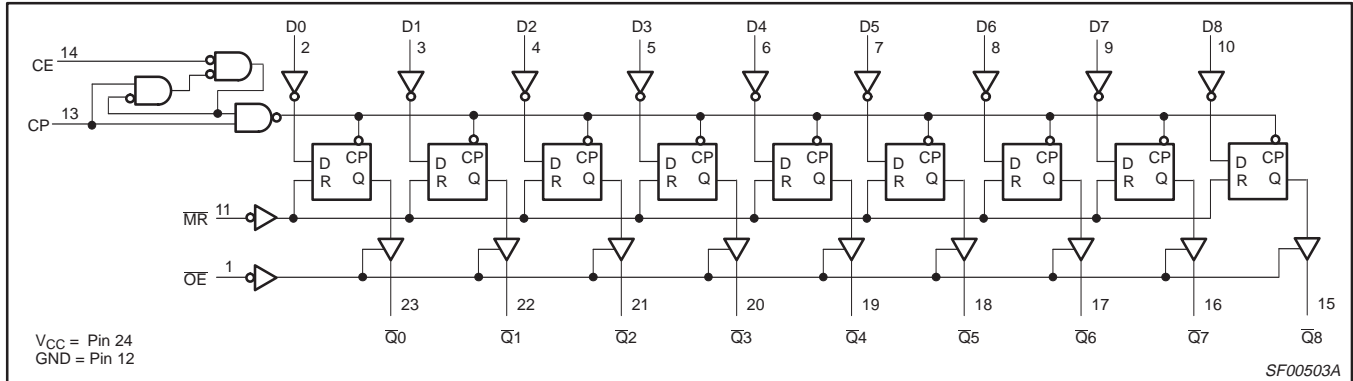
### LOGIC DIAGRAM FOR 74F823



Bus interface registers

74F821/822/823/824/825/826

LOGIC DIAGRAM FOR 74F824

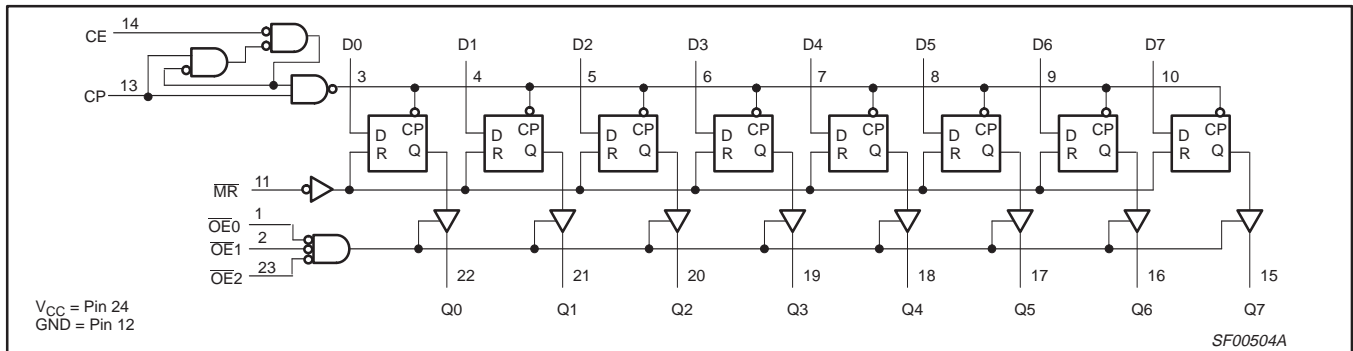


FUNCTION TABLE for 74F823 and 74F824

INPUTS					OUTPUTS		OPERATING MODE
					74F823	74F824	
OE	MR	CE*	CP	Dn	Q	Q̄	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Load and read data
L	H	L	↑	l	L	H	
L	H	H	X	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

- H = High-voltage level
- h = High state must be present one setup time before the low-to-high clock transition
- L = Low-voltage level
- l = Low state must be present one setup time before the low-to-high clock transition
- NC = No change
- X = Don't care
- Z = High impedance "off" state
- \* = Since CE input is sensitive to very short (<3ns) high-to-low-to-high going spikes while CP is high, users should avoid the use of decoders or other potentially glitch prone device on the CE input.
- ↑ = Low-to-high clock transition

LOGIC DIAGRAM FOR 74F825

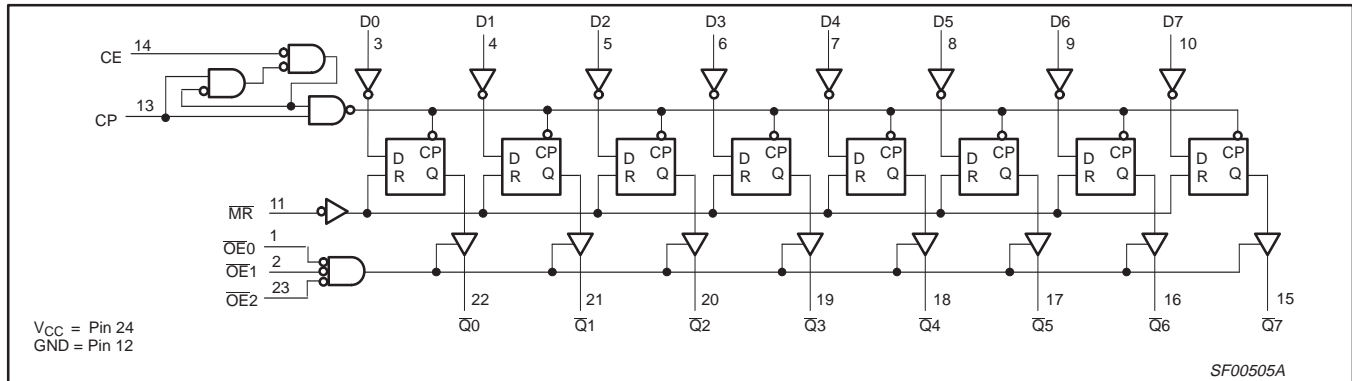




# Bus interface registers

# 74F821/822/823/824/825/826

## LOGIC DIAGRAM FOR 74F826



## FUNCTION TABLE FOR 74F825 AND 74F826

INPUTS					OUTPUTS		OPERATING MODE
					74F825	74F826	
OE <sub>n</sub>	MR	CE*	CP	D <sub>n</sub>	Q	Q̄	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Load and read data
L	H	L	↑	l	L	H	
L	H	H	X	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

- H = High-voltage level
- h = High state must be present one setup time before the low-to-high clock transition
- L = Low-voltage level
- l = Low state must be present one setup time before the low-to-high clock transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- \* = Since CE input is sensitive to very short (<3ns) high-to-low-to-high going spikes while CP is high, users should avoid the use of decoders or other potentially glitch prone device on the CE input.
- ↑ = Low-to-high clock transition

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in high output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in low output state	128	mA
T <sub>amb</sub>	Operating free-air temperature range	Commercial range	0 to +70
		Industrial range	-40 to +85
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

## Bus interface registers

## 74F821/822/823/824/825/826

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>Ik</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-24	mA
I <sub>OL</sub>	Low-level output current			64	mA
T <sub>amb</sub>	Operating free-air temperature range	Commercial range	0	+70	°C
		Industrial range	-40	+85	°C

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -15mA	±10%V <sub>CC</sub>	2.4		V
				±5%V <sub>CC</sub>	2.4		V
			I <sub>OH</sub> = -24mA	±10%V <sub>CC</sub>	2.0		V
				±5%V <sub>CC</sub>	2.0		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.55	V
				±5%V <sub>CC</sub>		0.42	0.55
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = 0.0V, V <sub>I</sub> = 7.0V			100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-20	μA	
I <sub>OZH</sub>	Off-state output current, high-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V			50	μA	
I <sub>OZL</sub>	Off-state output current, low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V			-50	μA	
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX	-100		-225	mA	
I <sub>CC</sub>	Supply current (total)	74F821, 74F822	I <sub>CCH</sub>	V <sub>CC</sub> = MAX	75	105	mA
			I <sub>CCL</sub>		75	105	mA
			I <sub>CCZ</sub>		75	115	mA
		74F823, 74F824	I <sub>CCH</sub>	V <sub>CC</sub> = MAX	65	100	mA
			I <sub>CCL</sub>		70	105	mA
			I <sub>CCZ</sub>		75	110	mA
		74F825, 74F826	I <sub>CCH</sub>	V <sub>CC</sub> = MAX	60	85	mA
			I <sub>CCL</sub>		60	90	mA
			I <sub>CCZ</sub>		65	95	mA

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

Bus interface registers

74F821/822/823/824/825/826

AC ELECTRICAL CHARACTERISTICS FOR 74F821/74F822/74F824/74F825/74F826

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>	Maximum clock frequency		Waveform 1	150	180		140		ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Qn or $\bar{Q}$ n	74F821, 74F825, 74F826	Waveform 1	4.0 4.0	6.5 6.0	8.5 8.5	4.0 3.5	9.5 9.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to $\bar{Q}$ n	74F822, 74F824	Waveform 1	4.5 4.5	6.5 6.5	9.0 9.0	4.5 4.5	10.0 9.0	ns
t <sub>PHL</sub>	Propagation delay $\bar{M}R$ to Qn or $\bar{Q}$ n	74F824 74F825, 74F826	Waveform 2	3.0	5.0	8.0	3.0	8.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\bar{O}E$ n to Qn or $\bar{Q}$ n		Waveform 4 Waveform 5	2.0 3.0	4.5 5.0	8.0 8.0	2.0 2.5	9.0 9.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\bar{O}E$ n to Qn or $\bar{Q}$ n		Waveform 4 Waveform 5	1.5 1.5	3.5 3.5	6.5 6.5	1.5 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS FOR 74F821/74F822/74F824/74F825/74F826

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t <sub>su</sub> (H) t <sub>su</sub> (L)	Setup time, high or low Dn to CP		Waveform 3	1.0 1.0			1.0 1.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, high or low Dn to CP		Waveform 3	2.0 2.0			2.0 2.0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse width, high or low		Waveform 1	3.5 3.5			4.0 4.0		ns
t <sub>su</sub> (H) t <sub>su</sub> (L)	Setup time, high or low, $\bar{C}E$ to CP	74F824, 74F825, 74F826	Waveform 3	0.0 2.0			0.0 2.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, high or low $\bar{C}E$ to CP		Waveform 3	0.0 3.0			0.0 3.5		ns
t <sub>w</sub> (L)	$\bar{M}R$ Pulse width, low		Waveform 2	4.5			4.5		ns
t <sub>rec</sub>	Recovery time, $\bar{M}R$ to CP		Waveform 2	2.5			2.5		ns

## Bus interface registers

## 74F821/822/823/824/825/826

## AC ELECTRICAL CHARACTERISTICS FOR 74F823

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
$f_{max}$	Maximum clock frequency	Waveform 1	150	180		140		130		ns
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to $Q_n$ or $\bar{Q}_n$	Waveform 1	4.0 4.0	6.5 6.0	8.5 8.5	4.0 3.5	9.5 9.0	4.0 3.5	10.0 9.0	ns
$t_{PHL}$	Propagation delay $\bar{M}R$ to $Q_n$ or $\bar{Q}_n$	Waveform 2	3.0	5.0	8.0	3.0	8.0	3.0	8.5	ns
$t_{PZH}$ $t_{PZL}$	Output enable time $OEn$ to $Q_n$ or $\bar{Q}_n$	Waveform 4 Waveform 5	2.0 3.0	4.5 5.0	8.0 8.0	2.0 2.5	9.0 9.0	2.0 2.5	11.0 9.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time $OEn$ to $Q_n$ or $\bar{Q}_n$	Waveform 4 Waveform 5	1.5 1.5	3.5 3.5	6.5 6.5	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns

## AC SETUP REQUIREMENTS FOR 74F823

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Dn to CP	Waveform 3	1.0 1.0			1.0 1.0		2.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low Dn to CP	Waveform 3	2.0 2.0			2.0 2.0		2.5 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, high or low	Waveform 1	3.5 3.5			4.0 4.0		4.0 4.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low, $\bar{C}E$ to CP	Waveform 3	0.0 2.0			0.0 2.0		0.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low $\bar{C}E$ to CP	Waveform 3	0.0 3.0			0.0 3.5		1.5 4.0		ns
$t_w(L)$	$\bar{M}R$ Pulse width, low	Waveform 2	4.5			4.5		4.5		ns
$t_{rec}$	Recovery time, $\bar{M}R$ to CP	Waveform 2	2.5			2.5		2.5		ns

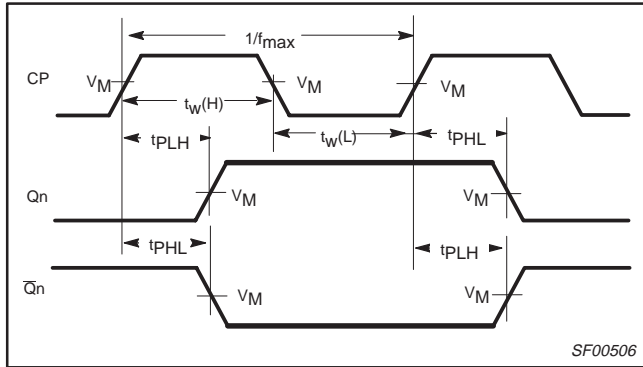
# Bus interface registers

# 74F821/822/823/824/825/826

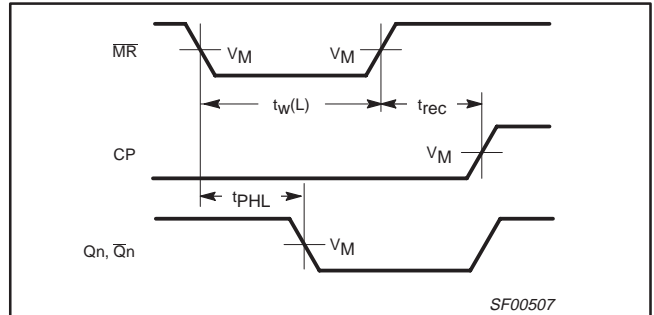
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .

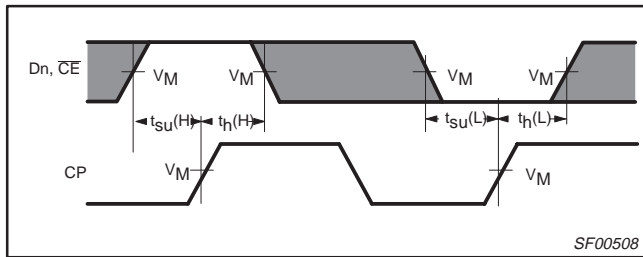
The shaded areas indicate when the input is permitted to change for predictable output performance.



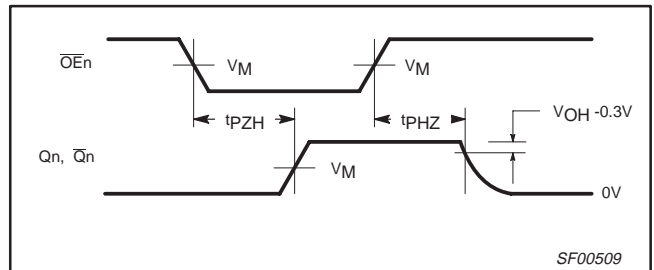
**Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency**



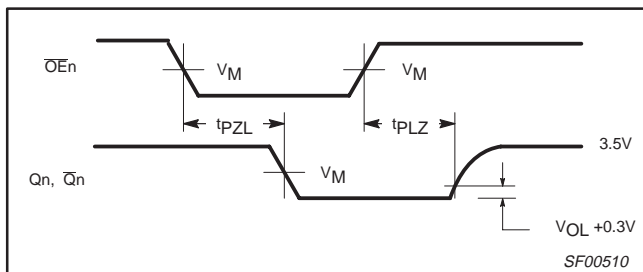
**Waveform 2. Master reset pulse width, master reset to output delay and master reset to clock recovery time**



**Waveform 3. Data setup time and hold times**



**Waveform 4. 3-State output enable time to high level and output disable time from high level**

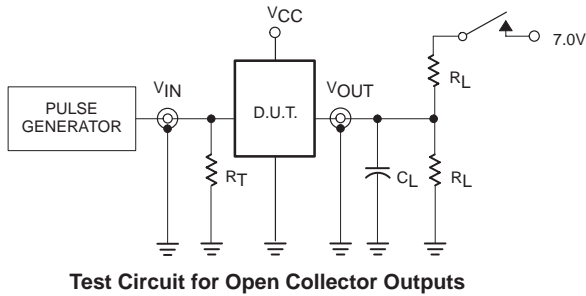


**Waveform 5. 3-State output enable time to low level and output disable time from low level**

# Bus interface registers

# 74F821/822/823/824/825/826

## TEST CIRCUIT AND WAVEFORMS

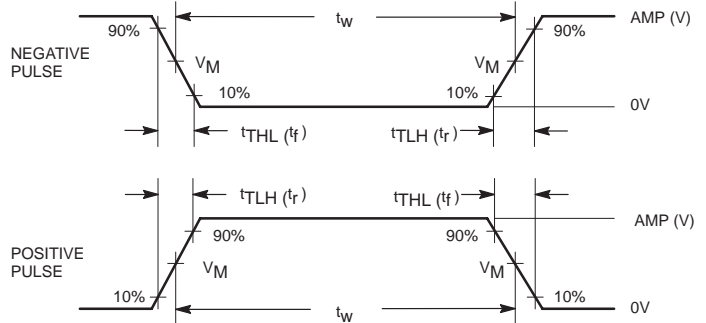


**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC electrical characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



**Input Pulse Definition**

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

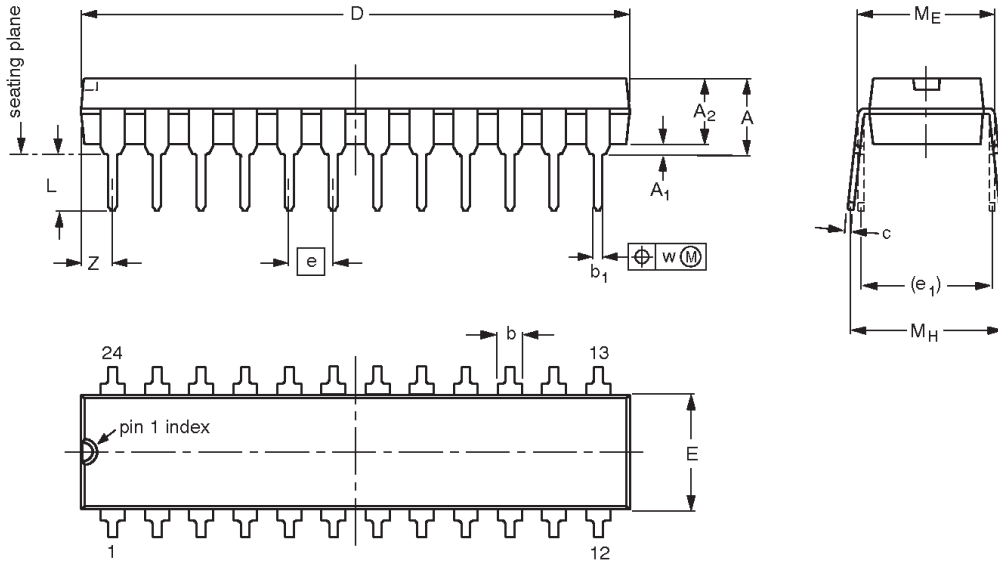
SF00128

Bus interface registers

74F821/822/823/824/825/826

DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

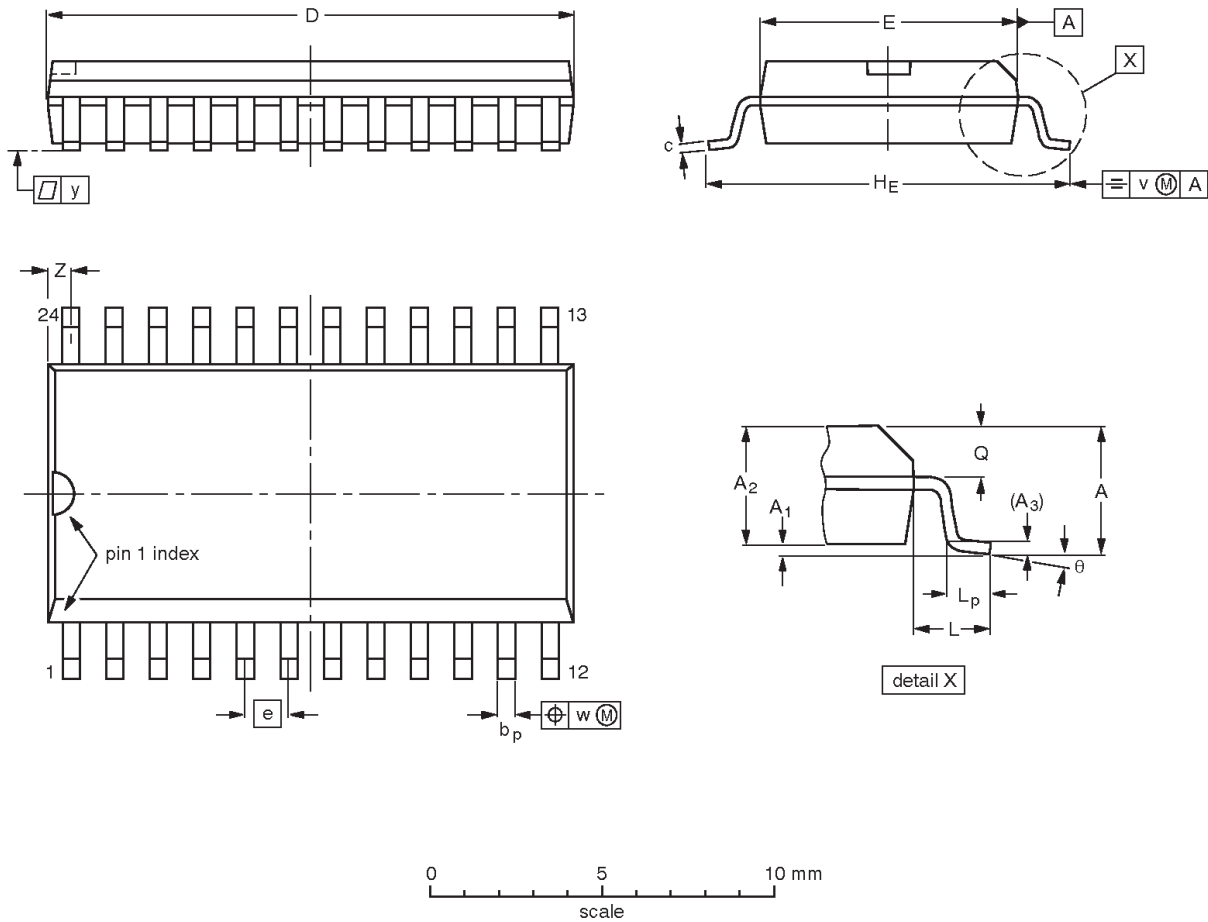
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

# Bus interface registers

# 74F821/822/823/824/825/826

**SO24:** plastic small outline package; 24 leads; body width 7.5 mm

**SOT137-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22



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# Bus interface registers

74F821/822/823/824/825/826

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## NOTES

## Bus interface registers

74F821/822/823/824/825/826

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
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